REMARKS

Claims 1 through 23 are pending in this application. Claims 1, 7, and 15 are the independent claims. Claims 1, 3, 7, 9, 11, 12, 15, 17, 18, 22 and 23 have been amended.

The Examiner has objected to the title of the invention indicating that a new title is required that is more clearly indicative of the invention to which the claims are directed. The Examiner has objected to the abstract of the disclosure because it is too short. The Examiner has objected to the disclosure of the invention because of minor grammatical informalities. The Examiner has objected to claims 5, 6. 7, 9, 11, 12, 15, 18, 22, and 23 due to minor claim informalities. The Examiner has rejected claims 1 through 23 under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992.

SPECIFICATION OBJECTIONS

The Examiner has objected to the title of the invention indicating that a new title is required that is more clearly indicative of the invention to which the claims are directed. The title has been amended to recite a "METHOD AND APPARATUS FOR EXECUTING A 32-BIT APPLICATION BY CONFINING THE APPLICATION TO A 32-BIT ADDRESS SPACE SUBSET IN A 64-BIT PROCESSOR" to overcome the objection. Therefore, Applicants believe the amended title overcomes the Examiner's objection and respectfully request that the objection be withdrawn.

The Examiner has objected to the abstract of the disclosure as being too short. The abstract has been amended to fall within the required number of words and to be in the required form to overcome the objection. Therefore, Applicants believe the amended abstract overcomes the Examiner's objection and respectfully request the objection be withdrawn.

The Examiner has objected to the disclosure of the invention because of minor grammatical informalities. The suggested changes have been made as evidenced by changes in the specification. Therefore, Applicants believe the specification amendments overcome the Examiner's objection and respectfully request the objection be withdrawn.

CLAIM OBJECTIONS

The Examiner has objected to claims 5, 6, 7, 9, 11, 12, 15, 18, 22, and 23 due to minor claim informalities. Claims 5, 6, 7, 9, 11, 12, 15, 18, 22, and 23 have been amended to incorporate the Examiner's suggested corrections to overcome the objection. Therefore, Applicants believe the above amendments have rendered the objection moot and respectfully request the objection be withdrawn.

REJECTIONS UNDER 35 U.S.C. § 102

The Examiner has rejected claims 1 through 23 under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992. Independent claims 1, 7 and 15 have been amended to overcome the rejection.

Claim 1 has been amended to include some of the elements from original claim 3 to recite, *inter alia*:

> "means for confining the application to a first bit size address space subset, said means for confining comprising:
> means for truncating generated address references of the second bit size to the first bit size; and
> means for extending to the second bit size the truncated generated address references based at least in part on a setting of a predetermined control signal."

Contrary to the Examiner's assertion in relation to the rejection of claim 10, ". . . extending to the second bit size the truncated generated address references based at least in part on a setting of a predetermined control signal" is not disclosed or suggested by Killian et al.. Specifically, the portion of Killian et al. (see column 17, lines 27 through 31) asserted by the Examiner as anticipating the predetermined control signal is incorrect. Rather, the asserted portion is more accurately analogized to the address space control flag, since it defines whether addresses are treated as 32-bit or 64-bit addresses. The predetermined control signal recited in claim 1 is used to define whether the truncated, 32-bit addresses are either zero extended or sign extended. There is no equivalent structure in Killian et al. that is used to explicitly specify whether the truncated 32-bit addresses are either zero extended or sign extended. Therefore, Applicants believe the above amendments have rendered the rejection moot and respectfully request the Section 102 rejection of claim 1, and the claims that depend therefrom, be withdrawn.

Claims 7 and 19 have been similarly amended to recite, *inter alia*: "extend(ing) the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of a predetermined control signal." For at least those reasons given above for claim 1, Applicants believe the above amendments have rendered the rejection of claims 7 and 15, and the claims that depend variously therefrom, moot and respectfully request the Section 102 rejection of be withdrawn.

Accordingly, Applicants believe that claims 1 through 23 are allowable over the applied art and respectfully request a notice of allowance to that effect be issued.

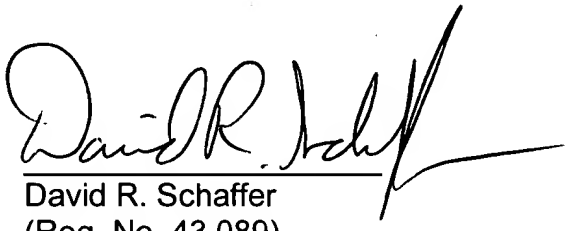
CONCLUSION

In view of the above remarks, the Applicants respectfully submit that the present case is in condition for allowance and request the Examiner issue a notice of allowance to that effect.

The commissioner is hereby authorized to charge any additional fees required under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to **Deposit Account No. 11-0600**.

The Examiner is invited to contact the undersigned at (202) 220-4263 to discuss any matter concerning this application.

Respectfully submitted,



Dated: April 14, 2003

David R. Schaffer
(Reg. No. 43,089)

KENYON & KENYON
1500 K Street, N.W., Suite 700
Washington, DC 20005
(202) 220-4200

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